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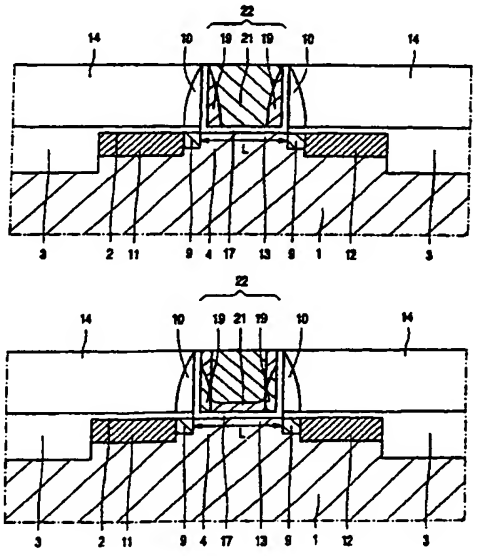
(54) Title: A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE



(57) Abstract: In a method of manufacturing a semiconductor device comprising a transistor having a gate (22) insulated from a channel (13) by a gate dielectric (17), which channel (13) is provided in an active region (4) of a first conductivity type provided at a surface (2) of a semiconductor body (1) and has a length L over which it extends between a source zone (11,9) and a drain zone (12,9) of a second conductivity type, the active region (4) of the first conductivity type is defined in the semiconductor body (1), and a dielectric layer (14) is applied which is provided with a recess at the area of the gate (22) planned to be provided at a later stage, in which recess an insulating layer is applied, forming the gate dielectric (17) of the transistor. Then, a first conductive layer and a second conductive layer are applied, the first conductive

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layer being relatively thin compared to the width of the recess, which first conductive layer and second conductive layer jointly form the gate (22) of the transistor and fill the recess in the dielectric layer (14). The gate comprises a central portion (21) and side end portions (19) positioned along either side of the central portion (21), which central portion (21) and side end portions (19) are in contact with the gate dielectric (17) and jointly establish a work function of the gate (22) varying across the length L of the channel (13).

A method of manufacturing a semiconductor device.

The invention relates to a method of manufacturing a semiconductor device comprising a semiconductor body which is provided at a surface with an active region of a first conductivity type, which active region is provided with a transistor having a gate insulated from a channel provided at the surface of the semiconductor body by a gate dielectric, the channel having a length over which it extends between a source zone and a drain zone of a second conductivity type provided in the semiconductor body, the gate comprising a central portion and side end portions positioned along either side of the central portion, which central portion and side end portions are in contact with the gate dielectric and jointly establish a work function of the gate varying across the length of the channel.

Such a method is known from US-A-5,466,958. In the known method, a first layer of polycrystalline silicon is deposited on a gate oxide layer present on the surface of the semiconductor body, which first layer of polycrystalline silicon is patterned by means of a lithographic technique and an etching treatment so as to form the central portion of the gate. A second layer of polycrystalline silicon is deposited and anisotropically etched so as to provide the central portion of the gate with side walls, which represent the side end portions of the gate.

A disadvantage of the known method is that the gate cannot be built up from the central portion and the side end portions in a length equal to the minimum feature size obtainable by means of a lithographic step, but is inevitably built up so as to have a length larger than the minimum lithographic feature size.

It is an object of the invention to provide a method of manufacturing a semiconductor device of the kind mentioned in the opening paragraph, which enables the formation of the gate in a length that is smaller than the length obtained in the known method and that may even be approximately equal to the minimum feature size obtainable by means of a lithographic step in special cases.

According to the invention, this object is achieved in that after the definition of the active region, a dielectric layer is applied which is provided with a recess at the area of the gate planned to be provided at a later stage, in which recess an insulating layer is applied, providing the gate dielectric of the transistor, after which a first conductive layer and a second conductive layer are applied, the first conductive layer being relatively thin compared to the width of the recess, which first conductive layer and second conductive layer jointly form the gate of the transistor and fill the recess in the dielectric layer.

As the gate is built up from the central portion and the side end portions in a length defined by the width of the recess in the dielectric layer, which recess is lithographically provided at an earlier stage of the process, the gate can be formed in a length that is smaller than the length obtained in the known method and that may even be approximately equal to the minimum feature size obtainable by means of a lithographic step in special cases.

The dielectric layer provided with the recess may be obtained by depositing the dielectric layer and subsequently etching it while using a mask exposing the area of the planned gate. In this way, the formation of the source zone and the drain zone needs to be carried out after the formation of the gate. The gate will hence be subjected to temperatures as high as approximately 1000°C, which are needed to electrically activate the as-implanted atoms and to repair the implantation damage brought about to the lattice of the semiconductor body. Exposure of the gate to such high temperatures imposes serious constraints on the choice of process-compatible gate materials. A preferred embodiment of the method in accordance with the invention is therefore characterized in that, prior to the application of the dielectric layer, a patterned layer is applied at the area of the planned gate, after which the source zone and the drain zone of the second conductivity type are formed in the semiconductor body while using the patterned layer as a mask, after which the dielectric layer is provided in such a way, that the thickness of the dielectric layer next to the patterned layer is substantially equally large or larger than the height of the patterned layer, which dielectric layer is removed over part of its thickness by means of a material removing treatment until the patterned layer is exposed, which patterned layer is removed, thereby forming the recess in the dielectric layer at the area of the planned gate.

MOS transistors with channel lengths scaled down to deep sub-micron levels may suffer from so-called short-channel effects. One of these short-channel effects is known as short-channel threshold-voltage reduction. Experimentally it is observed that, as the channel length decreases to less than about 1 μm, the threshold voltage of a MOS transistor

ultimately drops to a value below the long-channel value, which effect is referred to as short-channel threshold voltage reduction. The fraction of the depletion charge within the channel region, which is induced by the source zone and the drain zone, is insignificant for long-channel transistors, but becomes increasingly significant for short-channel transistors with the channel length approaching the sum of the widths of the depletion regions of the source zone and the drain zone. Consequently, less charge is needed to cause inversion, and the threshold voltage is reduced. In other words, the switching of short-channel transistors becomes less controlled by the gate.

Up to now, the short-channel threshold-voltage reduction could be kept within acceptable limits by reducing the junction depth of the source zone and the drain zone and increasing the channel dopant level. However, for MOS transistors with channel lengths approaching 0.1 μm this approach no longer works, because the suppression of the short-channel threshold-voltage reduction requires too high dopant levels in the channel, which leads to junction breakdown. An alternative approach for suppressing the short-channel threshold-voltage reduction is based on lateral grading of the work function of the gate. Hence, in order to compensate for a threshold-voltage reduction owing to short-channel effects, it is advantageous to vary the work function of the side end portions of the gate relative to the work function of the central portion of the gate.

One embodiment of the method in accordance with the invention is characterized in that, prior to the application of the second conductive layer, the first conductive layer is anisotropically etched until the gate dielectric at the area of the central portion of the gate to be provided at a later stage is exposed, thereby providing the side end portions of the gate, after which the second conductive layer is applied, thereby filling the recess and providing the central portion of the gate. In order to compensate for a short-channel threshold-voltage reduction, the first conductive layer is advantageously applied with a Fermi level lower than that of the second conductive layer for an n-channel transistor, whereas the first conductive layer is advantageously applied with a Fermi level higher than that of the second conductive layer for a p-channel transistor. It will be evident that several combinations of conductive materials, which may be selected from, for example, metals and semiconductor materials, are possible for the first conductive layer and the second conductive layer, each one of these combinations usually satisfying only one of the above-mentioned conditions, that is to say the condition for the n-channel MOS transistor or the condition for the p-channel MOS transistor. It is therefore advantageous to apply a layer of a semiconductor material of the second conductivity type as the second conductive layer, the

semiconductor material having a band gap, and to apply a layer of a conductive material having a Fermi level positioned approximately halfway the band gap of the semiconductor material as the first conductive layer. This enables both a p-channel transistor and an n-channel transistor to be manufactured using one common first conductive layer, which reduces the number of masks required for the manufacture of a semiconductor device comprising an n-channel transistor as well as a p-channel transistor by two. Obviously, several combinations of a semiconductor material and a conductive material are possible, which satisfy the condition that the Fermi level of the conductive material is positioned approximately halfway the band gap of the semiconductor material. However, in order to increase the compatibility with standard CMOS processing, it is advantageous to apply polycrystalline silicon or amorphous silicon as the semiconductor material of the second conductive layer and a material selected from the group comprising titanium nitride, tungsten and tantalum disilicide as the conductive material of the first conductive layer.

Another embodiment of the method in accordance with the invention is characterized in that a layer of a semiconductor material is applied as the first conductive layer, which layer is implanted with impurities of the second conductivity type substantially perpendicularly to the surface of the semiconductor body, thereby providing the central portion and the side end portions of the gate, which central portion is relatively heavily doped compared to the side end portions, after which the second conductive layer is applied, thus filling the recess. An appropriate selection of implantation conditions enables the central portion of the gate to be doped with impurities, while the side end portions of the gate remain at least substantially free from impurities.

In order to increase the compatibility with standard CMOS processing, the layer of semiconductor material is advantageously applied by depositing a layer comprising silicon such as polycrystalline silicon, amorphous silicon or polycrystalline Si_xGe_{1-x}, with x representing the fraction of silicon lying in the range between 0 and 1. The second conductive layer may be applied as a layer of a semiconductor material of the second conductivity type, which layer may comprise silicon, such as polycrystalline silicon, amorphous silicon or polycrystalline Si_xGe_{1-x}. However, the second conductive layer is advantageously applied as a layer comprising a metal. This enables both a p-channel transistor and an n-channel transistor to be manufactured using one common second conductive layer, which reduces the number of masks required for the manufacture of a semiconductor device comprising an n-channel transistor as well as a p-channel transistor by two. Metals intrinsically have a relatively low resistance compared to silicon and do not suffer from detrimental depletion

effects. In this respect, a low-resistance metal such as aluminum, tungsten, copper or molybdenum can be advantageously applied. If a metal is used, the second conductive layer is preferably applied as a double-layer consisting of a layer comprising the metal on top of a layer acting as adhesion layer and/or barrier layer. In this respect Ti may be applied as the adhesion layer and TiN or TiW as the barrier layer.

These and other aspects of the invention will be apparent from and be elucidated with reference to the embodiments described hereinafter and shown in the drawings. In the drawings:

Figs. 1 to 11 show in diagrammatic cross-sectional views successive stages in the manufacture of a semiconductor device comprising a transistor, using a first embodiment of the method in accordance with the invention.

Figs. 12 to 15 show in diagrammatic cross-sectional views successive stages in the manufacture of a semiconductor device comprising a transistor, using a second embodiment of the method in accordance with the invention.

Although the invention is illustrated hereinafter on the basis of a MOS transistor, it will be evident to those skilled in the art that the invention may also be advantageously applied in the manufacture of a MOS transistor with a floating gate, also referred to as floating gate transistor, or of CMOS and BICMOS integrated circuits known per se.

Figs. 1 to 11 show in diagrammatic cross-sectional views successive stages in the manufacture of a semiconductor device comprising a transistor, using a first embodiment of the method in accordance with the invention.

With reference to Fig. 1, a semiconductor body 1 of a first conductivity type, in the present example a silicon body of, for instance, p-type conductivity, is provided at a surface 2 with relatively thick oxide field insulating regions 3, which are at least partly recessed in the semiconductor body 1 and which define an active region 4 in which a transistor, in the present example an n-channel MOS transistor, is to be manufactured. The thick oxide insulating regions 3 are formed in a usual way by means of LOCOS (LOCal Oxidation of Silicon) or STI (Shallow Trench Isolation). Subsequently, the surface 2 of the semiconductor body 1 is provided with a layer 5 composed of, for instance, silicon oxide,

which is covered by a patterned layer 8 defining the area of a gate planned to be provided at a later stage of the process. In the present example, the patterned layer 8 is obtained by depositing a double-layer consisting of a first sub-layer 6 of, for instance, polycrystalline silicon which may be doped with a dopant such as phosphorus or possibly boron, and on top thereof, a second sub-layer 7 composed of, for instance, silicon nitride, and by patterning the double-layer for instance in a usual lithographic way. Instead of silicon nitride, any other suitable material such as, for instance, aluminum oxide or a combination of materials can be used. Instead of polycrystalline silicon, amorphous silicon or polycrystalline Si_xGe_{1-x} may be used, with x representing the fraction of silicon lying in the range between 0 and 1. It is to be noted, that the patterned layer may be a single layer as well, composed of polycrystalline silicon, amorphous silicon or polycrystalline Si_xGe_{1-x}, or any other suitable refractory material such as, for example, silicon nitride or aluminum oxide. Furthermore, the presence of the layer 5, which may have been advantageously applied in order to protect the semiconductor body against contamination, is not necessary. After applying the patterned layer 8, source/drain extensions 9 of a second, opposite conductivity type, in the present example n-type, are formed on opposite sides of the patterned layer 8 by means of a self-aligned implantation of a relatively light dose of, for instance, phosphorus or arsenic using the patterned layer 8 together with the oxide field insulating regions 3 as a mask.

Subsequently, the patterned layer 8 is provided with sidewall spacers 10 e.g. in a known way, for instance, by means of deposition and anisotropic etch-back of a silicon oxide layer (Fig. 2). After formation of the sidewall spacers 10, a highly-doped source zone 11 and drain zone 12 of the second conductivity type, in the present example n-type, are formed on opposite sides of the sidewall spacers 10 by means of a self-aligned implantation of a heavier dose of, for instance, phosphorus or arsenic using the oxide field insulating regions 3 together with the patterned layer 8 and the sidewall spacers 10 as a mask. It is to be noted, that a channel 13 is provided at the surface 2 of the semiconductor body 1 having a length L over which it extends between the extended source zone 11,9 and the extended drain zone 12,9.

With reference to Fig. 3, a relatively thick dielectric layer 14, in the present example composed of silicon oxide, is applied in such a way, that the thickness of the dielectric layer 14 next to the patterned layer 8 is substantially equally large or larger than the height of the patterned layer 8. Obviously, other suitable electrically insulating materials such as PSG (phosphosilicate glass) or BPSG (borophosphosilicate glass) may be used as well.

Subsequently, the dielectric layer 14 is removed over a part of its thickness until the patterned layer 8 is exposed (Fig. 4). This can be accomplished by means of, for example, chemical-mechanical polishing (CMP), e.g. using a commercially available slurry. During the material removing treatment, the second sub-layer 7, in the present example composed of silicon nitride, will act as a stopping layer.

In a next step (Fig. 5), the second sub-layer 7, composed of silicon nitride in the present example, is selectively removed with respect to the dielectric layer 14 and the sidewall spacers 10, both composed of silicon oxide in the present example, by means of, for instance, wet etching using a mixture of hot phosphoric acid and sulphuric acid.

With reference to Fig. 6, the first sub-layer 6 and the layer 5 are removed in two separate etching steps. The first sub-layer 6, in the present example composed of polycrystalline silicon, can be selectively removed by means of wet etching using, for instance, a hot KOH solution or by means of plasma etching with, for instance, a HBr/Cl_2 mixture. The layer 5, in the present example composed of silicon oxide, can be removed by means of a dip-etch using HF. In this way, the dielectric layer 14 is provided with a recess 15 at the area of the planned gate.

It is to be noted that the dielectric layer 14 provided with the recess 15 may also be obtained by depositing the dielectric layer 14 and subsequently etching the dielectric layer 14 using a mask exposing the area of the planned gate. In this way, the self-aligned implantation of the extended source zone 11,9 and the extended drain zone 12,9 would have to be carried out after formation of the gate. The gate will subsequently be subjected to temperatures as high as 1000 °C, which are needed to electrically activate the as-implanted atoms and to repair the implantation damage to the lattice of the semiconductor body 1. Exposure of the gate to such high temperatures imposes serious constraints on the choice of process-compatible gate materials.

As shown in Fig. 7, an insulating layer 16 is provided on all exposed surfaces, providing a gate dielectric 17 of the MOS transistor. The insulating layer 16 may be composed of silicon oxide, however, a dielectric material with a dielectric constant higher than that of silicon oxide, such as tantalum oxide, aluminum oxide or silicon nitride may be more favorable. If silicon oxide is to be applied for the gate dielectric 17, it may be obtained by means of, for instance, chemical vapor deposition or thermal oxidation of silicon. The high dielectric constant materials tantalum oxide, aluminum oxide and silicon nitride can be applied, for example, by means of chemical vapor deposition (CVD).

With reference to Fig. 8, a first conductive layer 18 is applied to the insulating layer 16 in a usual way, which first conductive layer 18 is relatively thin compared to the width of the recess 15 shown in Fig. 7. For example, in the case of a length L of the channel 13 of about 100 nm, the width of the recess 15 will be about 100 nm, whereas the thickness of the first conductive layer 18 will be in the range between about 15 and 40 nm. Moreover, in the case of a length L of the channel 13 of about 250 nm, the width of the recess 15 will be about 250 nm, whereas the thickness of the first conductive layer 18 will be in the range between about 40 and 100 nm.

The first conductive layer 18 is then anisotropically etched (Fig. 9), forming side end portions 19 of a gate 22 to be finally formed (see Fig. 11). The anisotropic etching treatment is continued until the gate dielectric 17 at the area of a central portion 21 of the gate 22 is exposed, which central portion 21 is provided in a next step (see Fig. 10). Alternatively, the first conductive layer 18 may be subjected to an anisotropic etching treatment until the gate dielectric 17 at the area of the central portion 21 has been approached up to about 10 nm, after which the actual exposure of the gate dielectric 17 is accomplished by means of an isotropic wet etching treatment.

With reference to Fig. 10, a second conductive layer 20 is applied in a usual way, thereby filling the recess 15 and providing the central portion 21, which central portion 21 is enclosed by the side end portions 19. The central portion 21 and the side end portions 19 of the gate 22 are in contact with the gate dielectric 17 and jointly establish a work function of the gate which varies across the length L of the channel 13, which channel 13 extends between the extended source zone 11,9 and the extended drain zone 12,9. In the present example, the work function of the side end portions 19 is varied relative to the work function of the central portion 21 in order to compensate for a threshold voltage reduction owing to short-channel effects. In case of an n-channel MOS transistor, this is achieved by applying the first conductive layer 18 with a Fermi level lower than that of the second conductive layer 20. It is understood by those skilled in the art that the first conductive layer 18 should be applied with a Fermi level higher than that of the second conductive layer 20 in order to obtain a similar effect for a p-channel MOS transistor. It will be evident that several combinations of conductive materials, which may be selected from, for example, metals and semiconductor materials, are possible for the first conductive layer and the second conductive layer, each one of these combinations usually satisfying only one of the above-mentioned conditions, that is to say the condition for the n-channel MOS transistor or the condition for the p-channel MOS transistor. It is therefore advantageous to apply the second conductive

layer 20 as a layer of a semiconductor material of the second conductivity type, namely the n-type in the case of an n-channel MOS transistor and the p-type in the case of a p-channel MOS transistor, the semiconductor material having a band gap, and to apply the first conductive layer 18 as a layer of a conductive material having a Fermi level positioned approximately halfway the band gap of the semiconductor material of the second conductive layer 20. This enables both a p-channel MOS transistor and an n-channel MOS transistor to be manufactured using one common first conductive layer 18, which reduces the number of masks required for the manufacture of a semiconductor device comprising an n-channel MOS transistor as well as a p-channel MOS transistor by two. In this respect, it is advantageous to apply polycrystalline silicon or amorphous silicon as the semiconductor material of the second conductive layer 20 and a material selected from the group comprising titanium nitride (TiN), tungsten (W) and tantalum disilicide ($TaSi_2$) as the conductive material of the first conductive layer 18. Anisotropic etching of titanium nitride may be carried out in, for example, a BCl_3 plasma, whereas anisotropic etching of tungsten and tantalum disilicide may be carried out in, for example, an SF_6 plasma. Obviously, other combinations of a semiconductor material and a conductive material are possible as well, provided the Fermi level of the conductive material is positioned approximately halfway the band gap of the semiconductor material. Doping of the semiconductor material may be carried out during deposition (in-situ) or after deposition.

With reference to Fig. 11, the second conductive layer 20 is shaped so as to complete the gate 22 of the MOS transistor. This can be achieved by means of, for example, etching using an oversized mask. In that case the conductive material of the gate 22 stretches out over the dielectric layer 14, which is coated with the insulating layer 16, to beyond the recess 15 shown in Fig. 7. It is however preferred to use a maskless process to remove the second conductive layer 20 until the insulating layer 16 is exposed, thereby forming the gate 22 which is recessed in the dielectric layer 14. An additional maskless removal of the insulating layer 16, the result of which is shown in Fig. 11, is not required, but can be beneficial in case the insulating layer 16 includes a high dielectric constant material. Maskless removal of either the second conductive layer 20 or the second conductive layer 20 and the insulating layer 16 is accomplished by means of, for example, chemical-mechanical polishing (CMP) using a commercially available slurry.

Figs. 12 to 15 show in diagrammatic cross-sectional views successive stages in the manufacture of a semiconductor device comprising a transistor, using a second embodiment of the method in accordance with the invention.

Fig. 12 shows the same situation as Fig. 8 except that the first conductive layer 18 is now applied as a layer of a semiconductor material, in the present example polycrystalline silicon, which layer of semiconductor material is relatively thin compared to the width of the recess 15 shown in Fig. 7. For example, in the case of a length L of the channel 13 of about 100 nm, the width of the recess 15 will be about 100 nm, whereas the thickness of the first conductive layer 18 will be in the range between about 15 and 40 nm. Moreover, in the case of a length L of the channel 13 of about 250 nm, the width of the recess 15 will be about 250 nm, whereas the thickness of the first conductive layer 18 will be in the range between about 40 and 100 nm. Amorphous silicon or polycrystalline Si_xGe_{1-x} may be used instead of polycrystalline silicon, with x representing the fraction of silicon lying between 0 and 1. Instead of one of the above-mentioned semiconductor materials, which all comprise silicon, a semiconductor material such as, for example, SiC or GaAs may be used. The first conductive layer 18 may be applied in a usual way by means of, for example, chemical vapor deposition.

In a next step (Fig. 13), the first conductive layer 18, in the present example a layer of polycrystalline silicon, is implanted with impurities of the second conductivity type, in the present example n-type impurities such as, for example, phosphorus (P) ions or arsenic (As) ions, substantially perpendicularly to the surface 2 of the semiconductor body 1 as depicted by arrows 23. It is to be noted that the above-mentioned implantation consists of an actual implantation of the atoms into the first conductive layer 18 followed by a short anneal or so-called drive-in step to electrically activate the as-implanted atoms. For example, phosphorus may be implanted at an energy lying in the range of about 1 to 15 keV and a dose of about 3.10^{13} to 3.10^{15} atoms/cm^2, and it may be annealed at a temperature of, for example, about 950°C for a time of, for example, about 10 seconds. On the other hand, arsenic may be implanted at an energy lying in the range of about 1 to 10 keV and a dose of about 3.10^{13} to 3.10^{15} atoms/cm^2, and it may be annealed at a temperature of, for example, about 950°C for a time of, for example, about 10 seconds. By carrying out the implantation substantially perpendicularly to the surface 2 of the semiconductor body 1, a central portion 21 and side end portions 19 positioned along either side of the central portion 21 are formed, which central portion 21 is relatively heavily doped compared to the side end portions 19. By an appropriate selection of implantation conditions it is possible to dope the central portion of the gate with impurities while keeping the side end portions of the gate at least substantially free from impurities. The central portion 21 and the side end portions 19, which are part of a gate 22 to be finally formed (see Fig. 15), are in contact with the gate dielectric 17 and jointly

establish a work function of the gate 22 varying across the length L of the channel 13, which channel 13 extends between the extended source zone 11,9 and the extended drain zone 12,9. In the present example, the work function of the side end portions 19 is varied relative to the work function of the central portion 21 in order to compensate for a threshold voltage reduction owing to short-channel effects. It is understood by those skilled in the art that boron (B) ions may be implanted in order to achieve a similar effect for a p-channel MOS transistor. Boron may be implanted at an energy lying in the range of about 0.5 to 5 keV and a dose of, for example, about 3.10^{13} to 3.10^{15} atoms/cm^2, and it may be annealed at a temperature of about 950°C for a time of, for example, about 10 seconds.

With reference to Fig. 14, a second conductive layer 20 is applied in a usual way, thereby filling the recess 15. The second conductive layer 20 may be applied as a layer of a semiconductor material of the second conductivity type, in the present example of the n-type. Polycrystalline silicon, amorphous silicon or polycrystalline Si_xGe_{1-x} may be used as the semiconductor material, with x representing the fraction of silicon lying between 0 and 1. Instead of one of the above-mentioned semiconductor materials, which all comprise silicon, a semiconductor material such as, for example, SiC or GaAs may be used. Doping of the semiconductor material may be carried out during deposition (in-situ) or after deposition. The second conductive layer 20 may, however, also be applied as a layer comprising a metal such as aluminum, tungsten, copper or molybdenum, or a combination of metals. This enables both a p-channel MOS transistor and an n-channel MOS transistor can be manufactured using one common second conductive layer 20, which reduces the number of masks required for the manufacture of a semiconductor device comprising an n-channel MOS transistor as well as a p-channel MOS transistor by two. If a metal or a combination of metals is used, the second conductive layer 20 is advantageously applied as a double-layer consisting of a layer comprising the metal or the combination of metals on top of a layer acting as adhesion layer and/or barrier layer. In this respect Ti may be applied as adhesion layer and TiN or TiW as barrier layer. It is clear that the above-mentioned implantation anneal imposes no constraints on the choice of materials for the second conductive layer 20, as this layer is applied after the implantation.

In a next step (Fig. 15), the first conductive layer 18 and the second conductive layer 20 are shaped so as to complete the gate 22 of the MOS transistor. This can be done by means of, for example, etching using an oversized mask. In that case the conductive material of the gate 22 stretches out over the dielectric layer 14, which is coated with the insulating layer 16, to beyond the recess 15 shown in Fig. 7. It is preferred, however,

to use a maskless process to remove the first conductive layer 18 and the second conductive layer 20 until the insulating layer 16 is exposed, thereby forming the gate 22 which is recessed in the dielectric layer 14. An additional maskless removal of the insulating layer 16, the result of which is shown in Fig. 15, is not required, but can be beneficial in case the insulating layer 16 includes a high dielectric constant material. Maskless removal of either the first conductive layer 18 and the second conductive layer 20 or the first conductive layer 18, the second conductive layer 20 and the insulating layer 16 is accomplished by means of, for example, chemical-mechanical polishing (CMP) using a commercially available slurry.

It will be apparent that the invention is not limited to the embodiments described above, but that many variations are possible to those skilled in the art within the scope of the invention. The side end portions of the gate, which are applied as sidewall spacers in the first embodiment described above, may each be built up from several sub-sidewall spacers, which jointly provide a work function varying across the side end portions. For the benefit of a p-channel transistor, the first conductive layer may also be applied as a layer of polycrystalline Si_xGe_{1-x} providing the central portion as well as the side end portions of the gate, which side end portions contain a relatively high fraction of germanium compared to the central portion. It is noted that, prior to the application of the first conductive layer and the second conductive layer, impurities may be introduced via the recess into the semiconductor body by means of, for example, ion implantation so as to provide for an impurity region for e.g. punchthrough suppression and/or threshold voltage adjustment. The surface layer, which is applied to the semiconductor body before the application of the patterned layer, may form the gate dielectric of the transistor instead of the insulating layer, which is applied after the provision of the recess in the dielectric layer. In that case, application of the insulating layer is omitted. Moreover, the source zone and the drain zone of the transistor can optionally be implanted without extensions. In the embodiments described above the active region is formed by a surface region of the original semiconductor body. Alternatively, the active region may represent a conventional p or n well, which is obtained by locally doping the original semiconductor body in a region adjoining its surface with a doping concentration suitable for providing an n-channel or p-channel transistor.

CLAIMS:

1. A method of manufacturing a semiconductor device comprising a semiconductor body which is provided at a surface with an active region of a first conductivity type, which active region is provided with a transistor having a gate insulated from a channel provided at the surface of the semiconductor body by a gate dielectric, the channel having a length over which it extends between a source zone and a drain zone of a second conductivity type provided in the semiconductor body, the gate comprising a central portion and side end portions positioned along either side of the central portion, which central portion and side end portions are in contact with the gate dielectric and jointly establish a work function of the gate varying across the length of the channel, characterized in that after the definition of the active region, a dielectric layer is applied which is provided with a recess at the area of the gate planned to be provided at a later stage, in which recess an insulating layer is applied, providing the gate dielectric of the transistor, after which a first conductive layer and a second conductive layer are applied, the first conductive layer being relatively thin compared to the width of the recess, which first conductive layer and second conductive layer jointly form the gate of the transistor and fill the recess in the dielectric layer.

2. A method as claimed in claim 1, characterized in that, prior to the application of the dielectric layer, a patterned layer is applied at the area of the planned gate, after which the source zone and the drain zone of the second conductivity type are formed in the semiconductor body while using the patterned layer as a mask, after which the dielectric layer is provided in such a way, that the thickness of the dielectric layer next to the patterned layer is substantially equally large or larger than the height of the patterned layer, which dielectric layer is removed over part of its thickness by means of a material removing treatment until the patterned layer is exposed, which patterned layer is removed, thereby forming the recess in the dielectric layer at the area of the planned gate.

3. A method as claimed in claim 1 or 2, characterized in that the work function of the side end portions of the gate is varied relative to the work function of the central portion

of the gate so as to compensate for a threshold voltage reduction owing to short-channel effects.

4. A method as claimed in claim 1, 2 or 3, characterized in that, prior to the application of the second conductive layer, the first conductive layer is anisotropically etched until the gate dielectric at the area of the central portion of the gate to be provided at a later stage is exposed, thereby providing the side end portions of the gate, after which the second conductive layer is applied, thereby filling the recess and providing the central portion of the gate.

5. A method as claimed in claim 4, characterized in that the first conductive layer is applied with a Fermi level lower than that of the second conductive layer if the transistor is applied as an n-channel transistor, whereas the first conductive layer is applied with a Fermi level higher than that of the second conductive layer if the transistor is applied as a p-channel transistor.

6. A method as claimed in claim 4 or 5, characterized in that a layer of a semiconductor material of the second conductivity type is applied as the second conductive layer, the semiconductor material having a band gap, and a layer of a conductive material having a Fermi level positioned approximately halfway the band gap of the semiconductor material is applied as the first conductive layer.

7. A method as claimed in claim 6, characterized in that the layer of the semiconductor material is applied by depositing a layer comprising silicon, whereas the conductive material is selected from the group comprising titanium nitride, tungsten and tantalum disilicide.

8. A method as claimed in claim 6 or 7, characterized in that the transistor is applied as an n-channel transistor and a further transistor is applied as a p-channel transistor, which n-channel transistor and p-channel transistor are manufactured using one common first conductive layer.

9. A method as claimed in claim 1, 2 or 3, characterized in that a layer of a semiconductor material is applied as the first conductive layer, which layer is implanted with

impurities of the second conductivity type substantially perpendicularly to the surface of the semiconductor body, thereby providing the central portion and the side end portions of the gate, which central portion is relatively heavily doped compared to the side end portions, after which the second conductive layer is applied thus filling the recess.

10. A method as claimed in claim 9, characterized in that a further layer of a semiconductor material of the second conductivity type is applied as the second conductive layer.

11. A method as claimed in claim 10, characterized in that the further layer of the semiconductor material is applied by depositing a layer comprising silicon.

12. A method as claimed in claim 9 as far as dependent on claims 2 and 3, characterized in that a layer comprising a metal is applied as the second conductive layer.

13. A method as claimed in claim 12, characterized in that the layer comprising the metal is applied as a double-layer consisting of a layer comprising the metal on top of a layer acting as adhesion and/or barrier layer.

14. A method as claimed in claim 12 or 13, characterized in that the metal is selected from the group comprising aluminum, tungsten, copper, and molybdenum.

15. A method as claimed in any one of claims 9 through 14, characterized in that the layer of the semiconductor material is applied by depositing a layer comprising silicon.

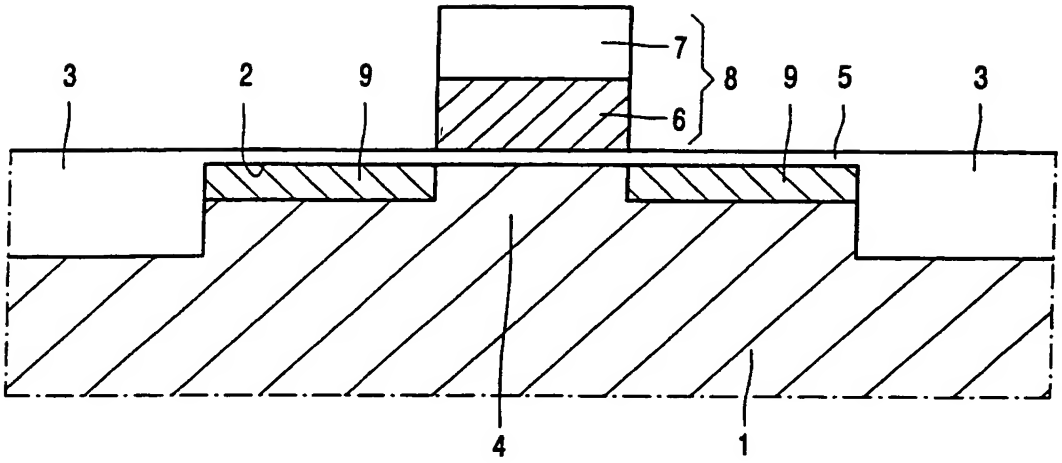


FIG. 1

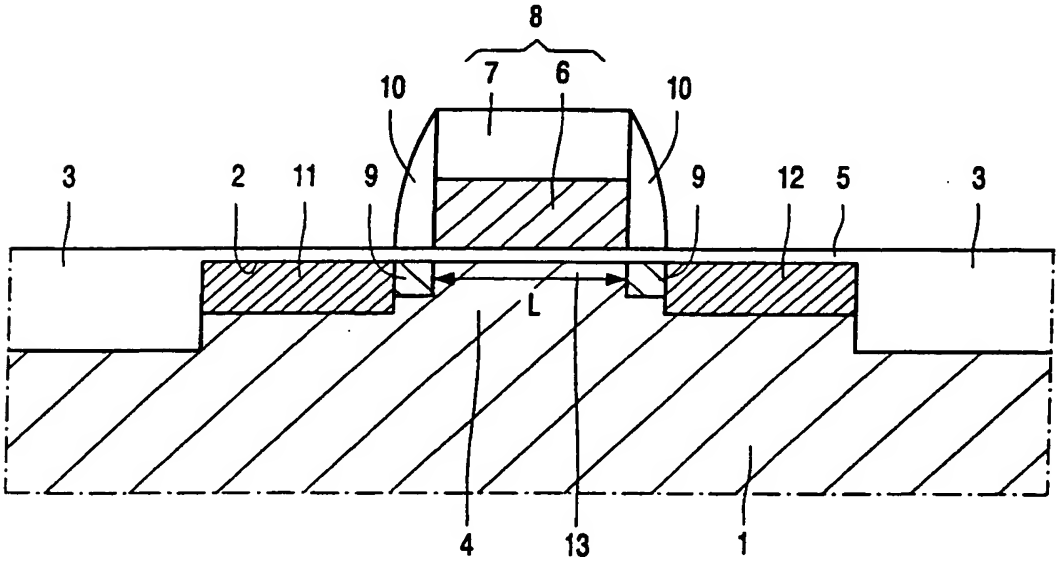


FIG. 2

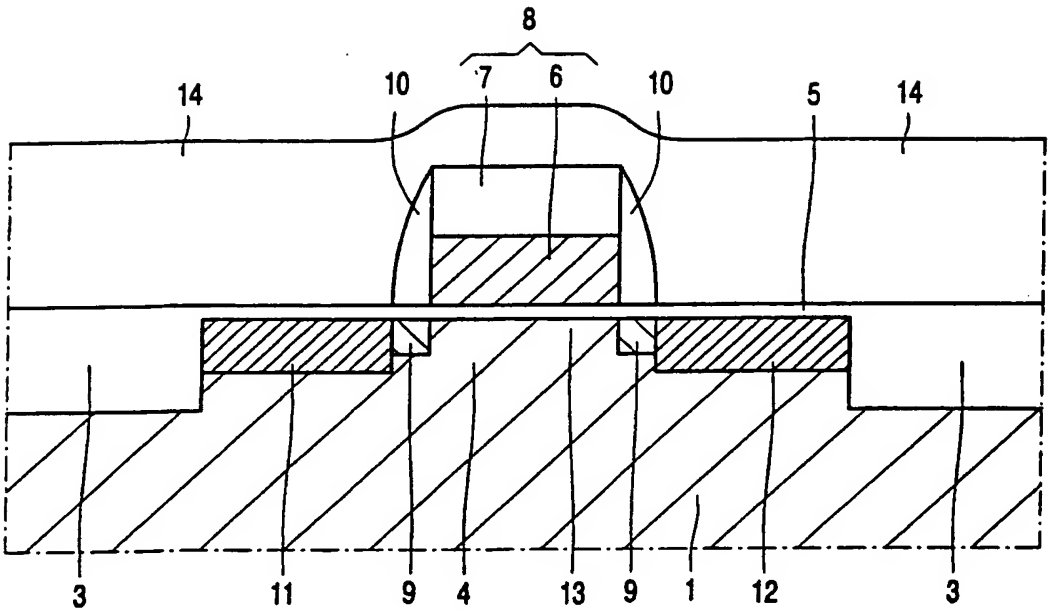


FIG. 3

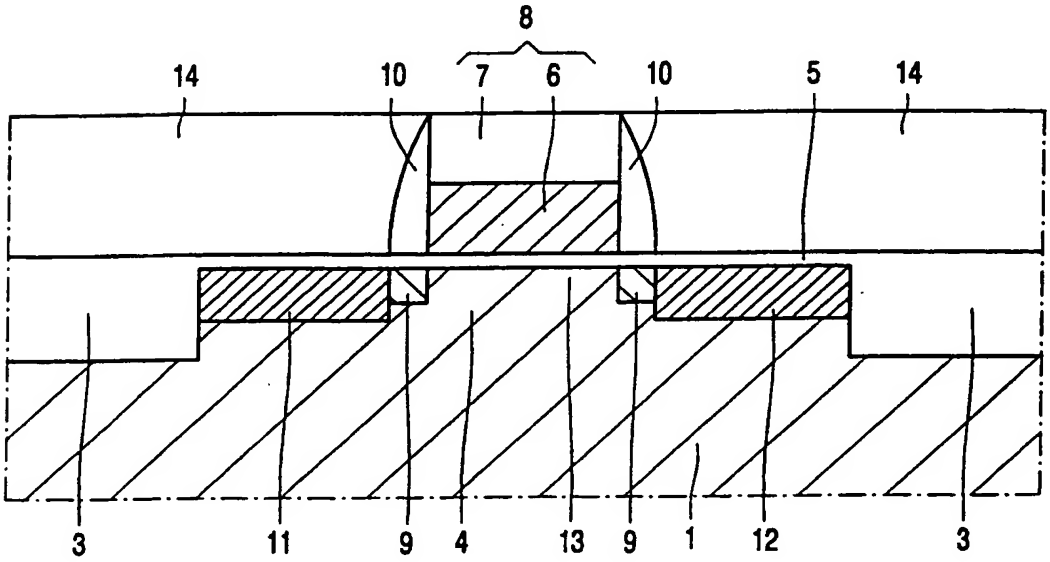


FIG. 4

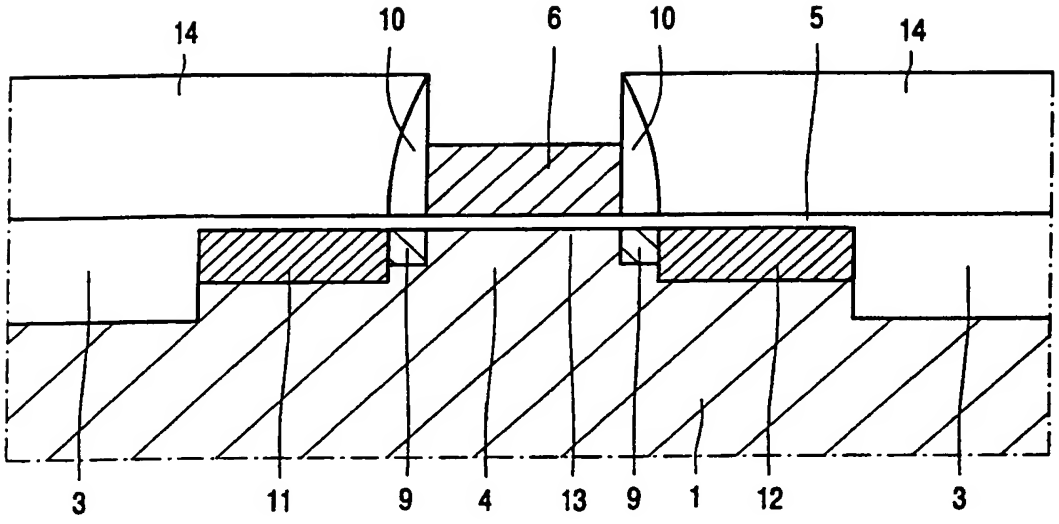
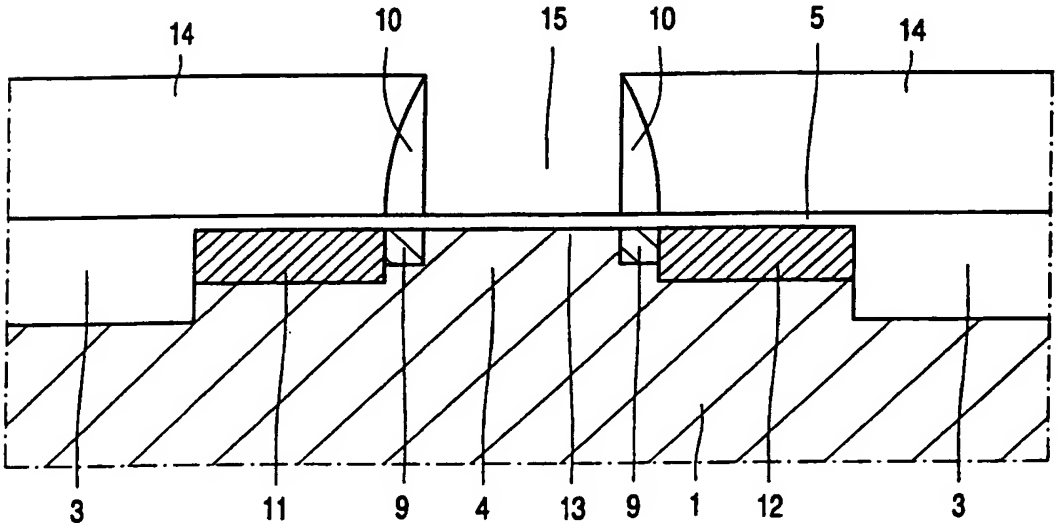


FIG. 5



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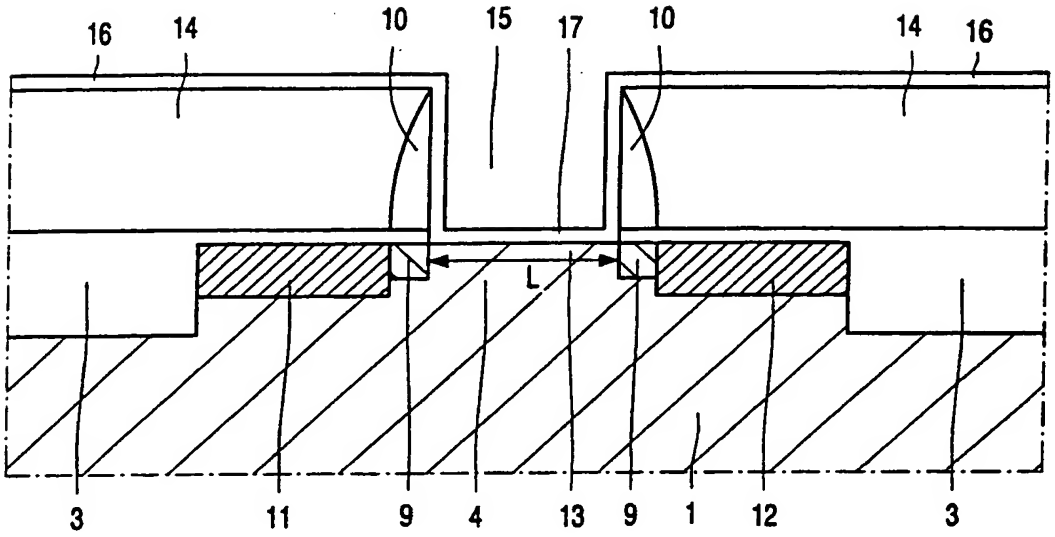
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FIG. 7

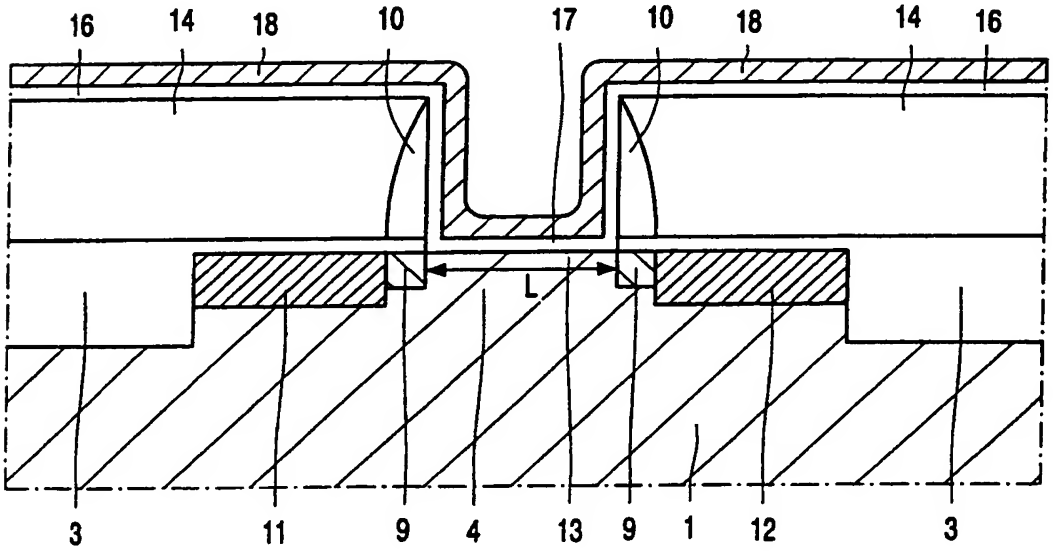
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FIG. 8

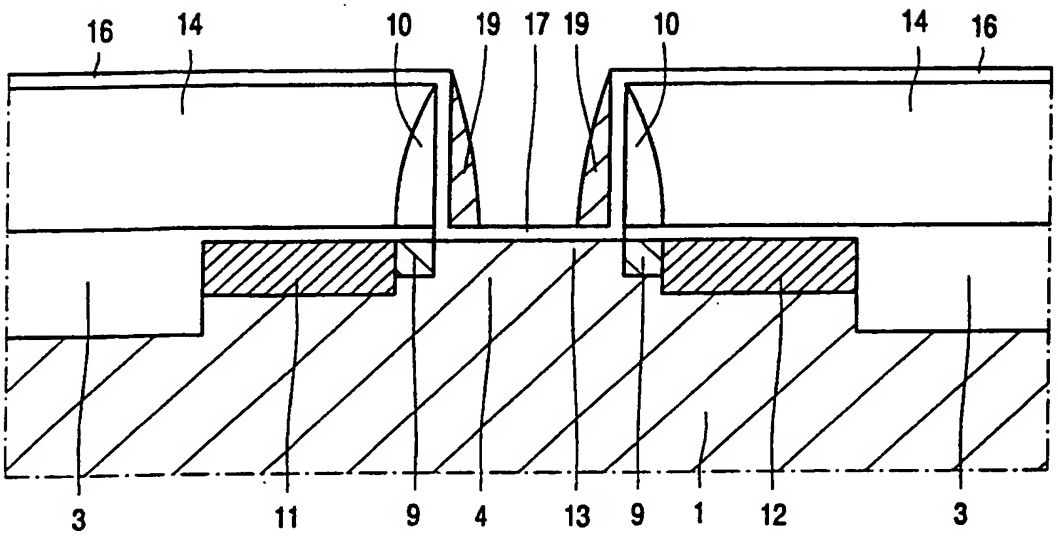
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FIG. 9

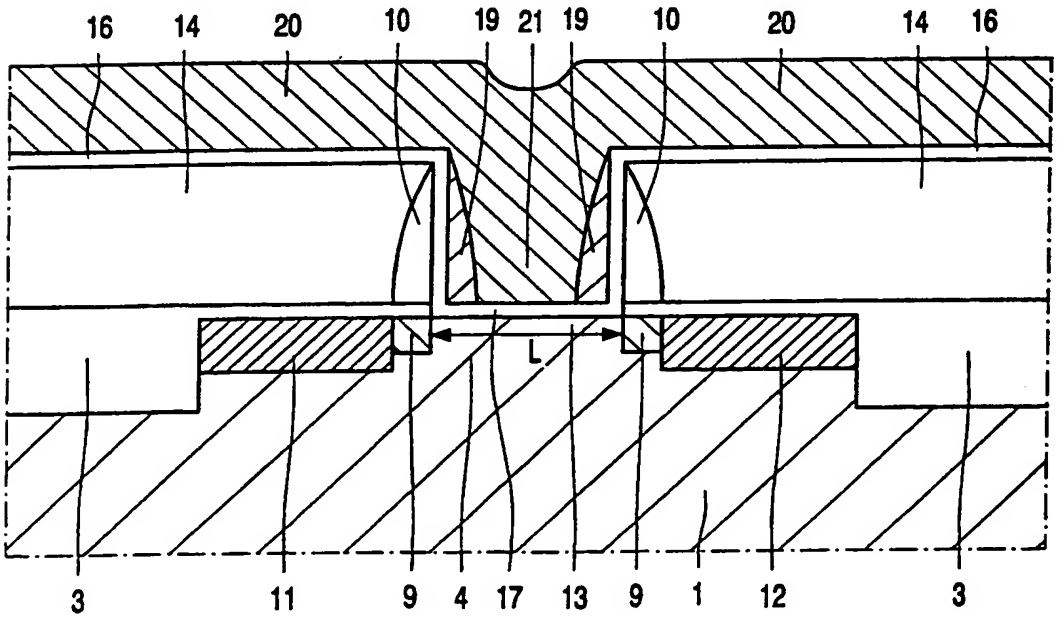
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FIG. 10

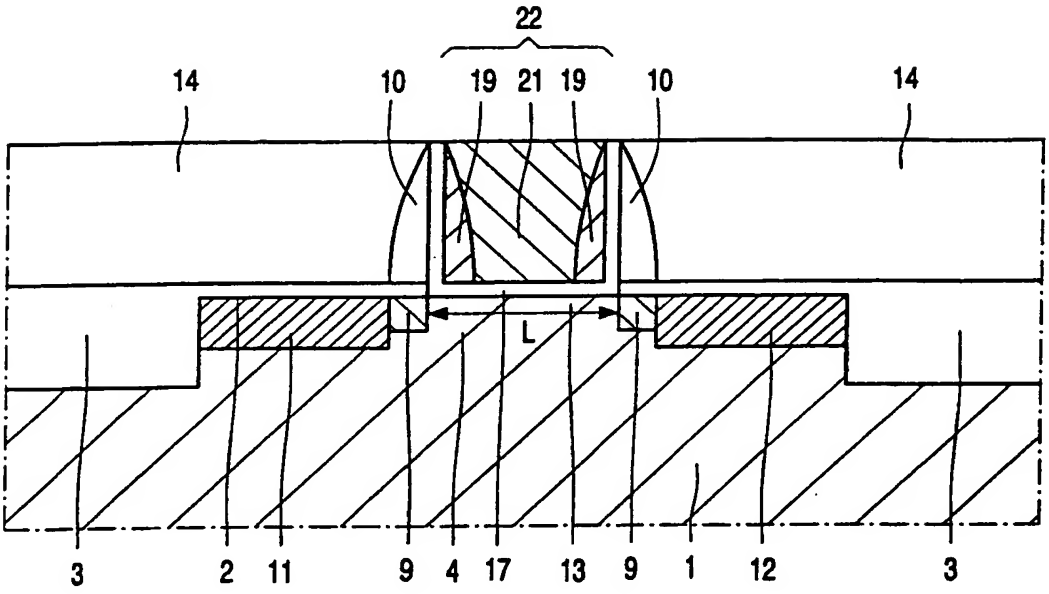

FIG. 11

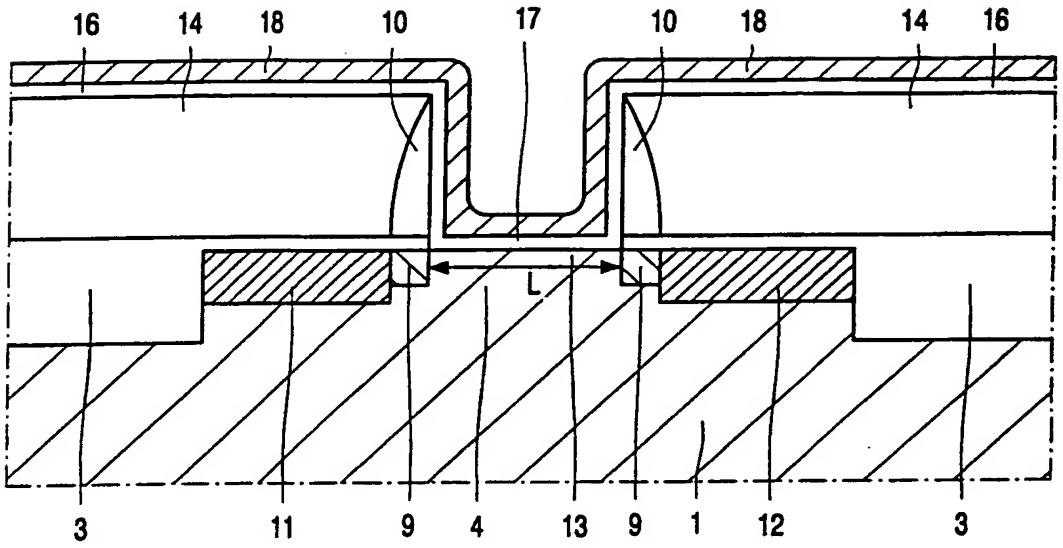
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FIG. 12

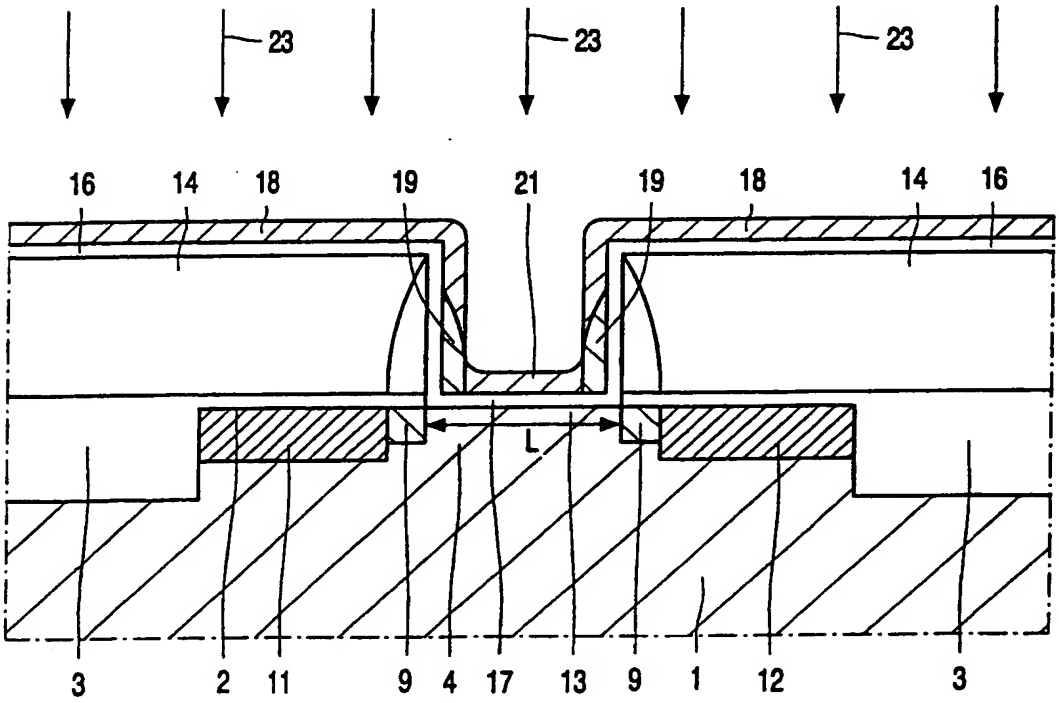
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FIG. 13

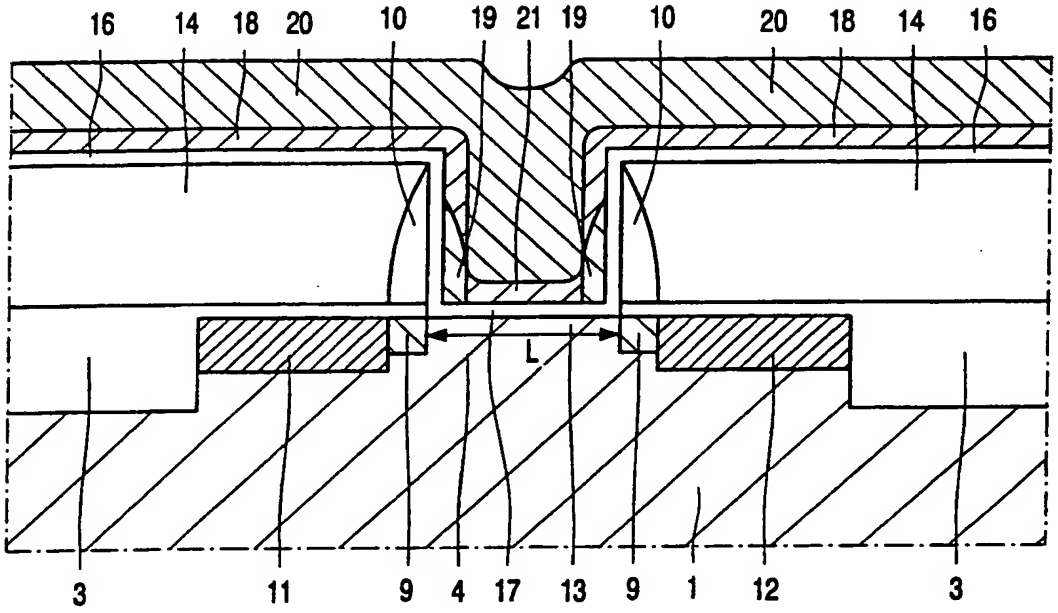
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FIG. 14

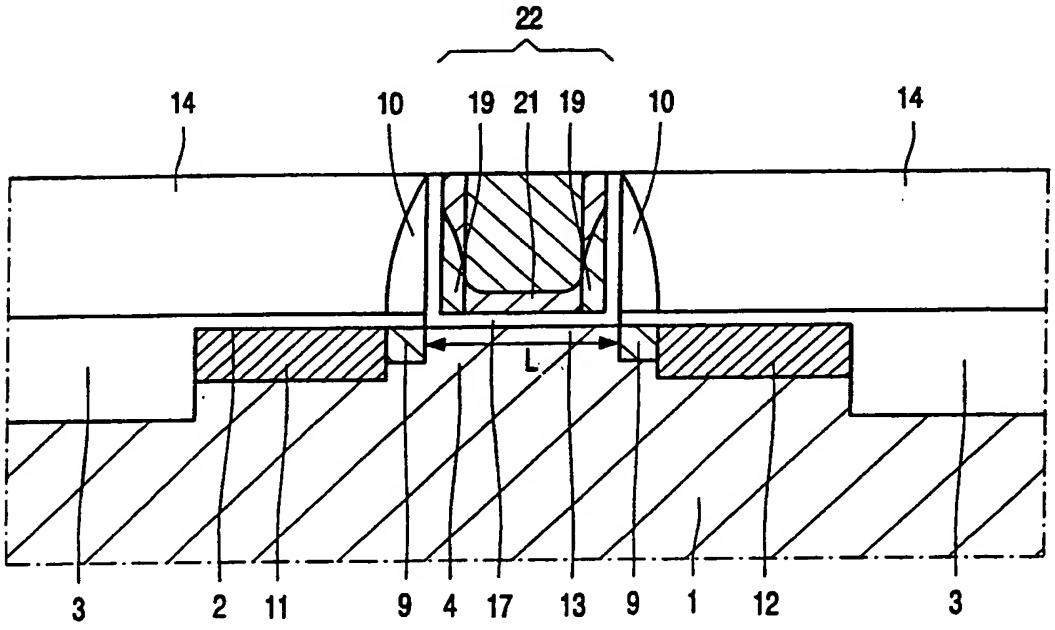
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FIG. 15

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(10) International Publication Number
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(72) Inventors: STOLK, Peter, A.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). PONOMAREV, Youri; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DUIJVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States *(national)*: JP, KR.

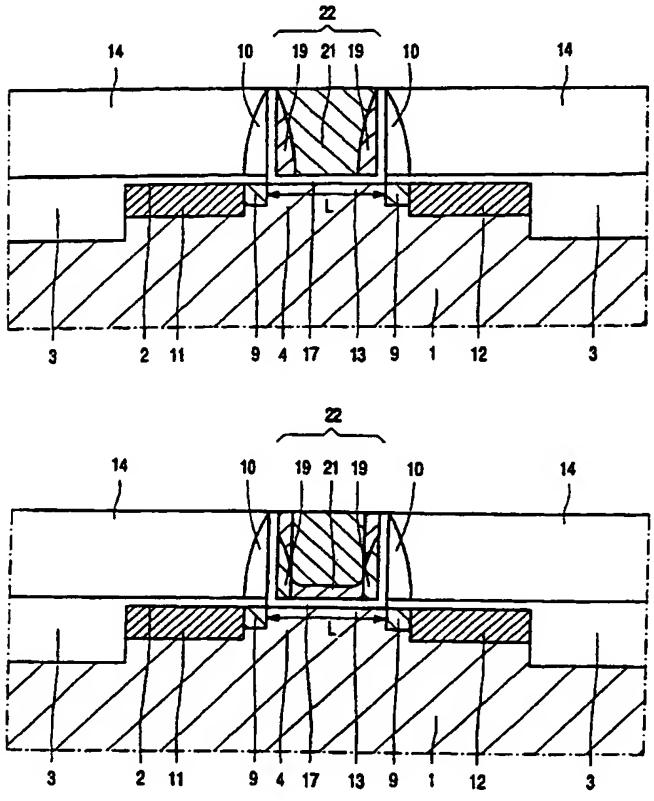
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published:
— *With international search report.*

(88) Date of publication of the international search report:
12 July 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD OF MANUFACTURING A VARIABLE WORK FUNCTION GATE MOSFET USING A DUMMY GATE



(57) Abstract: In a method of manufacturing a semiconductor device comprising a transistor having a gate (22) insulated from a channel (13) by a gate dielectric (17), which channel (13) is provided in an active region (4) of a first conductivity type provided at a surface (2) of a semiconductor body (1) and has a length L over which it extends between a source zone (11,9) and a drain zone (12,9) of a second conductivity type, the active region (4) of the first conductivity type is defined in the semiconductor body (1), and a dielectric layer (14) is applied which is provided with a recess at the area of the gate (22) planned to be provided at a later stage, in which recess an insulating layer is applied, forming the gate dielectric (17) of the transistor. Then, a first conductive layer and a second conductive layer are applied, the first conductive layer being relatively thin compared to the width of the recess, which first conductive layer and second conductive layer jointly form the gate (22) of the transistor and fill the recess in the dielectric layer (14). The gate comprises a central portion (21) and side end portions (19) positioned along either side of the central portion (21), which central portion (21) and side end portions (19) are in contact with the gate dielectric (17) and jointly establish a work function of the gate (22) varying across the length L of the channel (13).

WO 00/77828 A3

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/EP 00/05012

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L29/78 H01L29/49 H01L21/28

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 856 892 A (OKI ELECTRIC IND CO LTD) 5 August 1998 (1998-08-05) column 10, line 13 - line 45; figure 6 column 12, line 48 - line 54	1-7
Y	US 5 538 913 A (HONG GARY) 23 July 1996 (1996-07-23) figure 2	1-7
Y	PATENT ABSTRACTS OF JAPAN vol. 1998, no. 03, 27 February 1998 (1998-02-27) & JP 09 293862 A (SONY CORP), 11 November 1997 (1997-11-11) abstract -& US 6 001 698 A 14 December 1999 (1999-12-14) figure 4	2

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Date of the actual completion of the international search	Date of mailing of the international search report
23 January 2001	30/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Gélébart, J

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P,X	US 6 051 470 A (AN JUDY X ET AL) 18 April 2000 (2000-04-18) figures 1-12	1-7

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int. ional Application No
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